IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

re application of	:	Cornelis Hermanus Van Berkel, et al.
U.S. Serial No.	:	10/565,926
Filed	:	January 20, 2006
For	:	DEVICE AND METHOD FOR COMPOSING CODES
Group No.	:	2193
Examiner	:	Chat C. Do
Confirmation No.	:	9399

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

The Appellants have appealed to the Board of Patent Appeals and from the decision of the Examiner dated February 17, 2009, rejecting Claims 1-11. On May 18, 2009, the Appellants filed a Notice of Appeal that was received by the U.S. Patent and Trademark Office on May 22, 2009. The Notice of Panel Decision from Pre-Appeal Brief Review was mailed June 15, 2009. The Appellants respectfully submit this brief on appeal.

08/27/2009 JADD01 00000022 10565926
01 FC:1402 540.00 OP

TABLE OF CONTENTS

Real Party in Interest

The real party in interest, and assignee of this patent application, is ST-Ericcson, S.A.

An assignment from the inventors Cornelis Hermanus Van Berkel, Patrick Peter Elizabeth Meuwissen, and Ricky Johannes Maria Nas to KONNINKLIJKE PHILIPS ELECTRONICS, N.V. was recorded on January 20, 2006 in the Assignment Records of the United States Patent and Trademark Office at Reel 017517 and Frame 0046.

A subsequent assignment from KONNINKLIJKE PHILIPS ELECTRONICS, N.V. to NXP, B.V. was recorded on August 17, 2007 in the Assignment Records of the United States Patent and Trademark Office at Reel 019719 and Frame 0843.

Subsequent assignments from NXP, B.V. to ST Wireless, S.A., and from ST Wireless, S.A. to ST-Ericcson, S.A., have been made, but not yet recorded with the United States Patent and Trademark Office.

Related Appeals or Interferences

None. There are no appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this pending appeal.

Status of Claims

Claims 1-11 have been rejected pursuant to a Final Office Action dated February 17, 2009.

Claims 1-11 are presented for appeal.

A copy of Claims 1-11 is provided in Appendix A.

Status of Amendments after Final

The amendment to Claim 1 submitted after issuance of the Final Office Action dated February 17, 2009 has been denied entry by the examiner.

Summary of Claimed Subject Matter

The following general discussion provides background for understanding the invention. A concise explanation of the subject matter of the invention defined in each of the independent claims involved in the appeal is set forth below after the general discussion.

General Discussion

There is a variety of CDMA-like transmission standards, for example UMTS, CDMA2000, TD-SCDMA, and standards for other applications based on spread spectrum technology such as the global positioning system (GPS). Each of these standards uses a variety of different codes for synchronization, spreading and de-spreading, scrambling and de-scrambling, preambles and for other purposes. These codes are typically composed from a variety of basic codes, such as pseudo noise (PN) codes, Hadamard codes and OVSF codes. The basic codes often have parameters, for example generator polynomials, offsets and masks.[1]

A specific composite code can typically be generated by relatively simple and cheap hardware, like a linear feedback shift register (LFSR). A UMTS receiver, for example, then uses a variety of such generators to generate a specific composite code. However, this specific composite code is directly associated with the UMTS standard and therefore it is not generic.[2]

A code is also referred to as a sequence of symbols. A symbol is also referred to as a code chip or an element. A symbol may be a bit or another numerical value, either a real value or a complex value. A code vector is defined as a part of a complete code; the code vector comprises more than one symbol and is generated with a throughput of one vector per clock cycle.[3]

It is an object of the invention to provide a configurable generator of the kind set forth which is capable of generating composite-code vectors for a variety of transmission standards. This object is achieved by providing a device arranged to compose basic-code vectors into a

[1] See Appellants' published application, paragraph [0002].
[2] See Appellants' published application, paragraph [0003].
[3] See Appellants' published application, paragraph [0006].

composite-code vector and a method for composing basic-code vectors into a composite-code vector.[4]

FIG. 1 illustrates a device 100 arranged to combine basic-code vectors according to the invention. An input of the device 100 comprises a plurality of basic-code vectors 102a, 102b up to and including 102n. An output of the device 100 comprises a composite-code vector 104. The device 100 is capable of combining the basic-code vectors 102a, 102b up to and including 102n, under the control of a code configuration word 101. The use of the code configuration word 101 provides a certain degree of flexibility to the device 100, in the sense that the operation of the device 100 (determined by the functions which can be performed by the various components of the device 100) can be configured regularly.[5]

FIG. 2 illustrates various components of the device 100 arranged to combine a plurality of basic-code vectors 102a, 102b up to and including 102n, according to the invention. The device 100 comprises at least two weighted sum units 106a, 106b, and an add unit 110. Optionally, the device 100 comprises one or more pre-processing units 108a, 108b. Furthermore, a post-processing unit 112 may be provided, which can be coupled to a weighted sum unit 106a, 106b, and to the add unit 110.[6]

An input of the weighted sum units 106a, 106b receives a plurality of the basic-code vectors 102a, 102b up to and including 102n. The output of the weighted sum units 106a, 106b is provided as input to the add unit 110, or, if the device 100 comprises one or more pre-processing units 108a, 108b, as input to the pre-processing units. If the device 100 comprises one or more pre-processing units 108a, 108b, then the output of the pre-processing units is provided as input to the add unit 110. The output of the add unit 110 is the composite-code vector 104. Alternatively, if a post-processing unit 112 is deployed in the device 100, then the

[4] See Appellants' published application, paragraph [0008].
[5] See Appellants' published application, paragraph [0020].
[6] See Appellants' published application, paragraph [0021].

output of the add unit 110 is provided as input to the post-processing unit 112. In that case, the output of the post-processing unit 112 is the composite-code vector 104.[7]

Support for Independent Claims

Note that, per 37 C.F.R. § 41.37, only the independent claims are discussed in this section. The discussion of the independent claims in this section is for illustrative purposes and is not intended to affect the scope of the claims.

Claim 1 recites a device arranged to compose basic-code vectors into a composite-code vector.[8] The device includes at least two weighted sum units, each weighted sum unit being arranged to provide an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors.[9] The device also includes an add unit, the add unit being arranged to sum the intermediate-code vectors into the composite-code vector.[10] The weighted sum units being under the control of a first and a second configuration word.[11] The first and the second configuration word are deployed to configure the operations performed by the weighted sum units.[12]

---

[7] See Appellants' published application, paragraph [0022].
[8] See Appellants' published application, paragraph [0020], elements 100, 102*a*, 102*b* up to and including 102*n*, and 104.
[9] See Appellants' published application, paragraphs [0021] and [0022], elements 106*a*, 106*b* and 102*a*, 102*b* up to and including 102*n*.
[10] See Appellants' published application, paragraph [0022], elements 110 and 104.
[11] See Appellants' published application, paragraph [0022], elements 106*a*, 106*b* and 114*a*, 114*b*.
[12] See Appellants' published application, paragraph [0032], elements 114*a*, 114*b* and 106*a*, 106*b*.

Claim 11 recites a method for composing basic-code vectors into a composite-code vector.[13] The method includes (a) providing, by a vector processor, a first and a second intermediate-code vector, each of which is a weighted sum of a plurality of the basic-code vectors.[14] The method also includes (b) summing, by the vector processor, the intermediate-code vectors into a composite-code vector.[15] The method further includes (c) receiving, by the vector processor, a first and a second configuration word.[16] The method also includes (d) controlling, by the vector processor, step (a) with the first and the second configuration word.[17]

[13] See Appellants' published application, paragraph [0020], elements 100, 102*a*, 102*b* up to and including 102*n*, and 104.
[14] See Appellants' published application, paragraph [0022], elements 100 and 102*a*, 102*b* up to and including 102*n*.
[15] See Appellants' published application, paragraph [0022], elements 100 and 104.
[16] See Appellants' published application, paragraph [0022], elements 104 and 114*a*, 114*b*.
[17] See Appellants' published application, paragraph [0032], elements 100 and 114*a*, 114*b*.

Grounds of Rejection to be Reviewed on Appeal

1. Are Claims 1-10 unpatentable under 35 U.S.C. § 101 as being directed to non-statutory subject matter?

2. Are Claims 1-11 unpatentable under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,076,514, to *Erdogan et al.* (hereinafter referred to as "*Erdogan*")?

ARGUMENT

Legal Standard for Rejections under 35 U.S.C. § 101

MPEP §706.03(a) specifies that:

> 7.05.01 Rejection, 35 U.S.C. 101, Non-Statutory
> the claimed invention is directed to non-statutory subject matter because [1]
> Examiner Note
> In bracket 1, explain why the claimed invention is not patent eligible subject matter, e.g.,
> (a) why the claimed invention does not fall within at least one of the four categories of patent eligible subject matter recited in 35 U.S.C. 101 (process, machine, manufacture, or composition of matter); or
> (b) why the claimed invention is directed to a judicial exception to 35 U.S.C. 101 (i.e., an abstract idea, natural phenomenon, or law of nature) and is not directed to a practical application of such judicial exception (e.g., because the claim does not require any physical transformation and the invention as claimed does not produce a useful, concrete, and tangible result); or
> (c) why the claimed invention would impermissibly cover every substantial practical application of, and thereby preempt all use of, an abstract idea, natural phenomenon, or law of nature.

Legal Standard for Rejections under 35 U.S.C. § 102(e)

MPEP §2131 specifies that:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "When a claim covers several structures or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art." *Brown v. 3M*, 265 F.3d 1349, 1351, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) (claim to a system for setting a computer clock to an offset time to address the Year 2000 (Y2K) problem, applicable to records with

year date data in "at least one of two-digit, three-digit, or four-digit" representations, was held anticipated by a system that offsets year dates in only two-digit formats). See also MPEP § 2131.02. "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Note that, in some circumstances, it is permissible to use multiple references in a **35 U.S.C. 102** rejection. See **MPEP § 2131.01**.

Analysis of Examiner's Rejections

Ground of Rejection #1

Claims 1-10 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

The Appellants respectfully submit that the invention claimed in Claims 1-10:

1. does fall within at least one of the four categories of patent eligible subject matter recited in 35 U.S.C. 101; specifically, Claims 1-10 are directed to a particular machine;

2. is not directed to judicial exception to 35 U.S.C. 101, such an abstract idea, natural phenomenon, or law of nature; Claims 1-10 are directed to a practical application, i.e. the generation of composite-code vectors and the control of weighted sum units; and

3. does not impermissibly cover every substantial practical application of an abstract idea, natural phenomenon, or law of nature as the invention is not directed to an abstract idea, natural phenomenon, or law of nature.

Furthermore, the Appellants respectfully submit that a claimed process is surely patent-eligible under § 101 if: (1) it is tied to a particular machine or apparatus, or (2) it transforms a particular article into a different state or thing. A claimed process involving a fundamental

principle that uses a particular machine or apparatus would not pre-empt uses of the principle that do not also use the specified machine or apparatus in the manner claimed. And a claimed process that transforms a particular article to a specified different state or thing by applying a fundamental principle would not pre-empt the use of the principle to transform any other article, to transform the same article but in a manner not covered by the claim, or to do anything other than transform the specified article.[18]

Examiner suggests that, "Claims 1-10 cite a device for composing a composite-code vector in accordance with a mathematical algorithm. However, device claims 1-10 merely disclose series units with mathematical operations for composing the composite-code vector without disclosing the hardware components of the device."[19] However, the Appellants respectfully submit that Claims 1-10 are directed to a particular machine, i.e., a device arranged to compose basic-code vectors into a composite-code vector. Therefore, Claims 1-10 are directed to statutory subject matter.

In an attempt to further emphasize the fact that Claims 1-10 are directed to a particular machine, the Appellants requested that Claim 1 be amended to expressly recite that the elements are part of a vector processor.[20]

However, the Examiner indicated that the amendment to Claim 1 would not be entered because it would raise new issues that would require further consideration and/or search.[21] However, Claim 11 already recites a vector processor. Therefore, the amendment to Claim 1 does not raise new issues that would require further consideration and/or search as the added limitation of a vector processor should have already been considered and searched with regard to Claim 11. Accordingly, the Appellants respectfully submit that the Examiner erred in not entering the amendment to Claim 1.

---

[18] *In re Bilski*, 545 F.3d 943, 954 (Fed. Cir. 2008) (*en banc*).
[19] See Final Office Action mailed February 17, 2009, page 2, paragraph 4.
[20] See Appellants' response filed April 17, 2009.
[21] See Advisory Action mailed April 30, 2009.

The Examiner also responded to the Appellants' arguments by stating, "The examiner respectfully submits that the claims **might** not be statutory even if the claims are entered since just a vector processor itself would not provide sufficient structure to place the device claims into the statutory category."[22] Because the Examiner himself appears to be unclear as to what constitutes statutory subject matter and has not established that Claims 1-10 do in fact cover non-statutory subject matter, the Appellants respectfully request that the 35 U.S.C. § 101 rejection of Claims 1-10 be withdrawn.

Ground of Rejection #2

Claims 1-11 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,076,514, to Erdogan et al. (hereinafter referred to as "Erdogan").

For the reasons set forth below, the Appellants respectfully submit that the Examiner has not established a *prima facie* case of anticipation with respect to the claims of the Appellants' invention.

The cited reference is briefly discussed in relevant part for the rejection.

Claim 1:

The Appellants respectfully submit that *Erdogan* fails to show each and every limitation of Claim 1. Specifically, Claim 1 recites, "at least two weighted sum units, each weighted sum unit being arranged to provide an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors."

- The first summer and the second summer shown in FIG. 12 of *Erdogan* do not provide a weighted sum as recited in Claim 1.

[22] See Advisory Action mailed April 30, 2009. (Emphasis added by the Appellants.)

The Examiner continues to suggest that the first summer and the second summer shown in FIG. 12 of *Erdogan* are weighted sum units. For ease of reference, the first and second summers of *Erdogan* are described as follows:

> FIG. 12 illustrates a low complexity, efficient polyphase structure, according to an embodiment of the present invention. A first portion of the polyphase structure includes filters C_{11}, C_{12}, C_{13} and C_{14} for receiving inputs D_{11}, D_{12}, D_{21}, and D_{22} respectively. The outputs of filters C_{11}, C_{12}, C_{13} and C_{14} are then **combined by a first summer** and received by filter F_1. A second portion of the polyphase structure includes filters C_{21}, C_{22}, C_{23} and C_{24} for receiving inputs D_{11}, D_{12}, D_{21}, and D_{22} respectively. The outputs of filters C_{21}, C_{22}, C_{23} and C_{24} **are then combined by a second summer** and received by filter F_2. The outputs of filters F_1 and F_2 are combined by a third summer and received by a decimator structure. The decimator structure may include a Kth order integrator filter S_1, a downsampling function block N and a Kth order differentiator S_2. The decimator structure generates a digital sigma-delta output.[23]

As disclosed, the first and second summers of *Erdogan* simply sum the outputs of the filters. The Appellants are unable to find any mention of taking **weighted** sums in *Erdogan*. Furthermore, the Appellants also are unable to find any scaling or weighting with factors/coefficients by the first and second summers as suggested by the Examiner.[24]

The Examiner attempts to compensate for this deficiency in the teaching of *Erdogan* by suggesting that this is a reasonable broadest interpretation of the claims in light of the specification. However, as established above, the first and second summers of *Erdogan* simply sum the outputs of the filters and cannot be said to be **weighted** sum units. Therefore, the Examiner is not taking a reasonable broadest interpretation of the claims. The Examiner is simply ignoring an element of the claim, and the Appellants respectfully submit that all limitations of the claimed invention must be considered when determining patentability.[25]

In distinct contrast to *Erdogan*, Paragraph [0009] of the Appellants' published application discloses:

---

[23] See *Erdogan*, column 18, line 60-column 19, line 8. (Emphasis added by the Appellants.)
[24] See Final Office Action mailed February 17, 2009, page 7.
[25] *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994).

> The device according to the invention is provided with at least two weighted sum units, which are able to make a selection out of a plurality of incoming basic-code vectors by means of a weighted sum operation, under the control of a configuration word. The elements of this configuration word represent the weighting factors which are used to select or deselect a basic-code vector. The selected basic-code vectors are added together and the result of the weighted sum operation is then output as an intermediate-code vector. Subsequently, the intermediate-code vectors are added together by an add unit and output as a composite-code vector. The ability to make selections out of a plurality of incoming basic-code vectors and to add intermediate-code vectors into a composite-code vector, together with the ability to configure the operations of the functional units of the device by means of configuration words, increases the flexibility of the device significantly. This flexibility is needed to support a variety of transmission standards.[26]

Accordingly, even if one were to take a reasonable broadest interpretation of the claims in light of the specification as suggested by the Examiner, the outputs of the first and second summers of *Erdogan* still cannot be said to be **weighted** sum units.

The Examiner responds by stating, "the claims do not provide an explicit definition that is distinct from the cited reference by Erdogan."[27] The Appellants respectfully submit that a person of ordinary skill in the art would recognize the distinction between a weighted sum as recited in Claim 1 and a simple sum as performed by *Erdogan*. Furthermore, the Appellants respectfully submit that claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art.[28] Again, the Examiner is not taking a reasonable broadest interpretation of the claims, but is simply choosing to ignore an element of the claim.

- The first and second summers of *Erdogan* do not relate to standards and codes. Therefore, their outputs cannot be said to be an intermediate-code vector.

Furthermore, the Examiner continues to suggest that the output of the first and second summers of *Erdogan* is an intermediate-code vector which is a weighted sum of a plurality of the

[26] See Appellants' published application, paragraph [0009].
[27] See Advisory Action mailed April 30, 2009.

basic-code vectors. However, the first and second summers of *Erdogan* relate to analog to digital conversion (ADC). The first and second summers of *Erdogan* do not relate to standards and codes. Therefore, their outputs cannot be said to be an intermediate-code vector.

The Examiner also appears to suggest that the claims do not explicitly exclude interpreting A/D conversion as codes. First, the Appellants respectfully submit that one of ordinary skill in the art would interpret an intermediate-code vector as excluding A/D conversion. Second, claims are to be interpreted in light of the specification, and Paragraphs [0002] to [0009] of the Appellants' application clearly excludes interpreting an intermediate-code vector to include A/D conversion. For ease of reference, the sections pertaining to the filtered digital signal input and output of the first and second summers of *Erdogan* are set forth below:

> Another aspect of the present invention relates to Analog to Digital Conversion (ADC), which is **a process of sampling a continuous-time analog signal in time and mapping these time samples into a digital sequence with finite levels**. ADC refers to discretization of an input analog signal in both time and magnitude. For example, Sigma Delta converters provide high resolution analog to digital conversion. The high resolution may be achieved through over-sampling of an input signal at a rate higher than its bandwidth. ...
>
> An embodiment of the present invention is directed to a polyphase combiner and sigma-delta decimator block structure. ...
>
> FIG. 6 illustrates an analog to digital converter, according to an embodiment of the present invention. Analog signals are converted into digital signals by AID Converters by various methods, which may include Sigma-Delta A/D conversion. For high performance Sigma-Delta A/D conversion, an input analog signal may be sampled into a 2-bit (in some cases one bit or other number of bits) high-rate digital signal by Analog Sigma-Delta block 610. The digital signal is then down-sampled and converted into a high resolution (e.g., 16-bit) and lower rate digital signal by a Digital Sigma-Delta Decimator block 620. As shown in FIG. 6, Analog Sigma-Delta block 610 generates a two-bit digital output, D_1 and D_2. **Both D_1 and D_2 are binary signals with rate R. For example, D_1 carries a sampled signal with quantization noise and D_2 carries quantization noise cancellation information.** The Digital Sigma-Delta

[28] *In re Marosi*, 710 F.2d 799, 802-03, 218 U.S.P.Q. 289, 292 (Fed. Cir. 1983).

> Decimator 620 combines D_1 and D_2 and then decimates the combination by a factor M. ...
>
> FIG. 12 illustrates a low complexity, efficient polyphase structure, according to an embodiment of the present invention. **A first portion of the polyphase structure includes filters C_{11}, C_{12}, C_{13} and C_{14} for receiving inputs D_{11}, D_{12}, D_{21}, and D_{22} respectively. The outputs of filters C_{11}, C_{12}, C_{13} and C_{14} are then combined by a first summer and received by filter F_1. A second portion of the polyphase structure includes filters C_{21}, C_{22}, C_{23} and C_{24} for receiving inputs D_{11}, D_{12}, D_{21}, and D_{22} respectively. The outputs of filters C_{21}, C_{22}, C_{23} and C_{24} are then combined by a second summer and received by filter F_2.** The outputs of filters F_1 and F_2 are combined by a third summer and received by a decimator structure. The decimator structure may include a Kth order integrator filter S_1, a downsampling function block N and a Kth order differentiator S_2. The decimator structure generates a digital sigma-delta output.[29]

Thus, the first and second summers of *Erdogan* provide a sum of filtered binary signals and do not relate to standards and codes. A sum of filtered binary digital signals is not an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors.

The Examiner appears to suggest that the claims do not explicitly exclude the digital data outputs of the first and second summers and that these outputs can be considered as codes. However, in distinct contrast to *Erdogan*, the Appellants' published application discloses:

> There is a variety of CDMA-like transmission standards, for example UMTS, CDMA2000, TD-SCDMA, and standards for other applications based on spread spectrum technology such as the global positioning system (GPS). Each of these standards uses a variety of different codes for synchronization, spreading and de-spreading, scrambling and de-scrambling, preambles and for other purposes. These codes are typically composed from a variety of basic codes, such as pseudo noise (PN) codes, Hadamard codes and OVSF codes. The basic codes often have parameters, for example generator polynomials, offsets and masks.[30]
>
> A specific composite code can typically be generated by relatively simple and cheap hardware, like a linear feedback shift register (LFSR). A UMTS receiver, for example, then uses a variety of such generators to generate a specific

[29] See *Erdogan*, column 17, line 3-column 19, line 8. (Emphasis added by the Appellants.)
[30] See Appellants' published application, paragraph [0002].

composite code. However, this specific composite code is directly associated with the UMTS standard and therefore it is not generic.[31]

Configurable vector processors can be equipped with code generators, so that they are capable of handling different standards and codes. Furthermore, they can be arranged to provide support for related functions such as cyclic redundancy check (CRC). A configurable vector processor would then be equipped with a plurality of generators which generate basic codes in vector format. However, a disadvantage of such a configurable vector processor is that it cannot provide a composite code which is dependent on such basic codes. This is necessary if the configurable vector processors should be flexible enough to support a variety of CDMA-like standards.[32]

The device according to the invention is provided with at least two weighted sum units, which are able to make a selection out of a plurality of incoming basic-code vectors by means of a weighted sum operation, under the control of a configuration word. The elements of this configuration word represent the weighting factors which are used to select or deselect a basic-code vector. The selected basic-code vectors are added together and the result of the weighted sum operation is then output as an intermediate-code vector. Subsequently, the intermediate-code vectors are added together by an add unit and output as a composite-code vector. The ability to make selections out of a plurality of incoming basic-code vectors and to add intermediate-code vectors into a composite-code vector, together with the ability to configure the operations of the functional units of the device by means of configuration words, increases the flexibility of the device significantly. This flexibility is needed to support a variety of transmission standards.[33]

Again, claims are to be interpreted in light of the specification, and Paragraphs [0002] to [0009] of the Appellants' application clearly excludes interpreting a sum of filtered binary digital signals as an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors.

---

[31] See Appellants' published application, paragraph [0003].
[32] See Appellants' published application, paragraph [0004].
[33] See Appellants' published application, paragraph [0009].

Therefore, the Appellants respectfully submit that *Erdogan* fails to describe, teach or suggest "at least two weighted sum units, each weighted sum unit being arranged to provide an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors" as set forth in independent Claim 1. Thus, the Appellants respectfully submit that the Examiner has failed to establish a *prima facie* case of anticipation.

Accordingly, the Appellants respectfully submit that Claim 1 is not anticipated by *Erdogan*.

Claim 11:

Independent Claim 11 recites limitations analogous to the novel limitations emphasized above in traversing the rejection of Claim 1 and, therefore, also is patentable over *Erdogan*.

Dependent Claims

Dependent Claims 2-10 depend from independent Claim 1 and include all the limitations of Claim 1. As such, the Appellants respectfully submit that dependent Claims 2-10 also are not anticipated by *Erdogan*.

CONCLUSION

For the reasons set forth above, The Appellants respectfully submit that the rejections are improper and request the rejections under § 101 and § 102(e) be withdrawn.

REQUESTED RELIEF

Accordingly, the Board is respectfully requested to reverse the outstanding rejections of Claims 1-11 and return this application to the Examiner for allowance.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Munck Carter Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER, LLP

Date: 8/24/2009

Robert D. McCutcheon
Registration No. 38,717

P.O. Box 802432
Dallas, Texas 75380
(972) 628-3600 (main number)
(972) 628-3616 (fax)
E-mail: *rmcutcheon@munckcarter.com*

ATTORNEY FOR APPELLANT

APPENDIX A

CLAIMS APPENDIX

1. (Previously Presented) A device arranged to compose basic-code vectors into a composite-code vector, the device comprising:

at least two weighted sum units, each weighted sum unit being arranged to provide an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors;

an add unit, the add unit being arranged to sum the intermediate-code vectors into the composite-code vector;

the weighted sum units being under the control of a first and a second configuration word, and

wherein the first and the second configuration word are deployed to configure the operations performed by the weighted sum units.

2. (Previously Presented) A device according to claim 1, wherein a pre-processing unit is coupled to at least one of the weighted sum units and to the add unit, the pre-processing unit being arranged to perform additional operations on the intermediate-code vector, and the pre-processing unit being under the control of a third and a fourth configuration word, wherein the third and the fourth configuration word are deployed to configure the additional operations on the intermediate-code vector.

3. (Previously Presented) A device according to claim 1, wherein a post-processing unit is coupled to the add unit, the post-processing unit being arranged to perform additional operations on the composite-code vector, and the post-processing unit being under the control of a fifth configuration word, wherein the fifth configuration word is deployed to configure the additional operations on the composite-code vector.

4. (Previously Presented) A device according to claim 1, wherein the weighted sum units are arranged to calculate a bit-wise addition of at least two basic-code vectors.

5. (Previously Presented) A device according to claim 2, wherein the pre-processing unit is arranged to erase, repeat and reorder the elements of the intermediate-code vector.

6. (Previously Presented) A device according to claim 2, wherein the pre-processing unit is arranged to apply a mask on the intermediate-code vector.

7. (Previously Presented) A device according to claim 3, wherein the post-processing unit is arranged to perform a conditional negation of the composite-code vector.

8. (Previously Presented) A device according to claim 1, wherein the weighted sum units and the add unit are arranged to be configured during a configuration stage of the operation of the device.

9. (Previously Presented) A device according to claim 2, wherein the pre-processing unit is arranged to be configured during a configuration stage of the operation of the device.

10. (Previously Presented) A device according to claim 3, wherein the post-processing unit is arranged to be configured during a configuration stage of the operation of the device.

11. (Previously Presented) A method for composing basic-code vectors into a composite-code vector, the method comprising the steps of:

(a) providing, by a vector processor, a first and a second intermediate-code vector, each of which is a weighted sum of a plurality of the basic-code vectors;

(b) summing, by the vector processor, the intermediate-code vectors into a composite-code vector;

(c) receiving, by the vector processor, a first and a second configuration word; and

(d) controlling, by the vector processor, step (a) with the first and the second configuration word.

APPENDIX B

EVIDENCE APPENDIX

U.S. Patent No. 7,076,514, to *Erdogan et al.* ("*Erdogan*") found on pages 4-7 of the Office Action (dated September 15, 2008), and found on pages 3-8 of the Final Office Action (dated April 30, 2009).

APPENDIX C

RELATED PROCEEDINGS APPENDIX

None